MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2016/2017

EEE 3156 DIGITAL SYSTEMS

(EE Group)

17 OCTOBER 2016
2.30 p.m - 4.30 p.m
(2 Hours)

INSTRUCTION TO STUDENT

1. This Question paper consists of 5 pages including cover page with 4 Questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1:

(a) Using 5 units of two-input lookup tables (LUT), design the following function f. Please include the contents programmed in the lookup tables.

$$f(a, b, c) = \bar{a}b + ac + \bar{b}\bar{c}$$

[5 marks]

(b) A PAL is shown in Figure 1.1.

(i) Determine the equation of the output signal, f as shown in Figure 1.1.

[3 marks]

(ii) Implement the logic circuit as shown in Figure 1.1 using 3 units of three-input lookup tables only.

[5 marks]

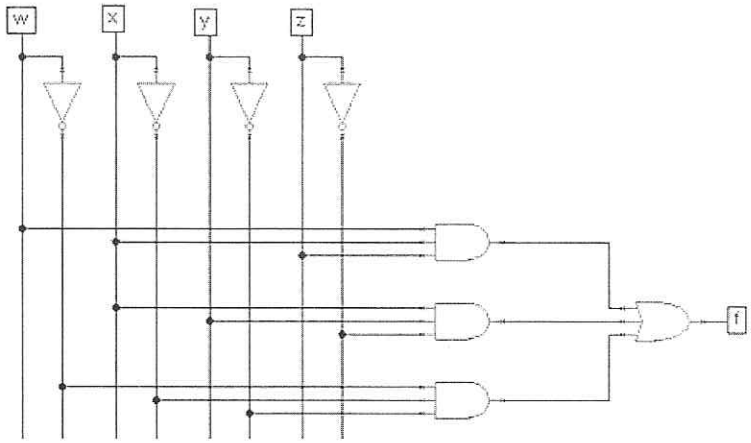

Figure 1.1

(iii) Simplify the following logic function using K-map and implement it using the programmable gate-array template as shown in Figure 1.2.

$$f(a, b, c, d) = \sum m(0,1,4,5,6,7,8,9,14,15)$$

[12 marks]

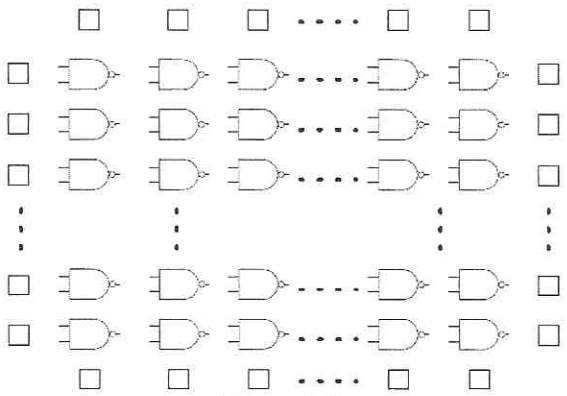

Figure 1.2

Continued ...

Question 2:

Refer to the state diagram of a sequential circuit shown in Figure 2.

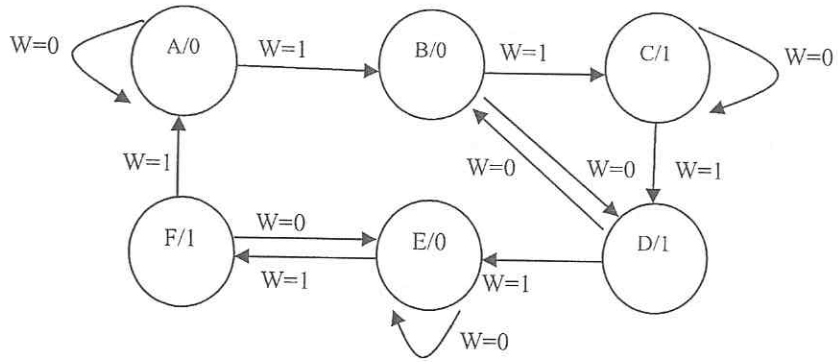

Figure 2

(a) Construct the state table of the sequential circuit. [6 marks]

(b) Construct the state assigned/transition table. [6 marks]

(c) Compute the simplified equations of the sequential circuit. [8 marks]

(d) From part (c), design the sequential circuit using logic gates and D flip-flops. [5 marks]

Continued ...

Question 3:

(a) A non-pipelined processor consists of five process stages. The execution time required for each stage is shown in Table 3a.

Table 3a

Stage	Execution time (ns)
Instruction fetch (IF)	50
Instruction decoding (ID)	40
Operand fetch (OF)	40
Execution (EX)	50
Write-back (WB)	50

(i) Compute the instruction latency of the non-pipelined processor.

[2 marks]

(ii) Compute the total time needed to execute 20 instructions.

[2 marks]

(iii) If pipelining is implemented on the processer, what is the new instruction latency of the pipelined processor? Assume pipelining method adds 2ns overhead to each execution stage.

[2 marks]

(iv) Compute the total time needed for the pipelined processor to execute 20 instructions.

[2 marks]

(v) From part (ii) & (iv), what is the average time to execute 1 instruction for non-pipelined and pipelined processor.

[2 marks]

(vi) Based on part (iv), calculate the speedup ratio obtained from the pipelined processor compared to the non-pipelined processor.

[2 marks]

(b) Refer to the reservation table of a pipelined processor in Table 3b.

Table 3b: Reservation table of a pipelined processor

	1	2	3	4	5	6	7
Stage 1	X					X	X
Stage 2		X	X				
Stage 3				X			
Stage 4					X		

(i) State the forbidden list and identify the collision vector.

[3 marks]

(ii) Construct the state diagram.

[8 marks]

(iii) Compute the minimum average latency, (MAL).

[2 marks]

Continued ...

Question 4:

(a) A five-stage pipelined microprocessor executed the instructions below.
i1: SUB R9, R8, R7
i2: ADD R5, R6, R9
i3: SUB R7, R9, R7
i4: ADD R9, R9, R5

State three types of data hazards in these instructions and explain them briefly.

[6 marks]

(b) Refer to the block diagram in Figure 4a. Given that the data delay at A= 20 μs, B = 25μs, D = 22μs, clock delay at C = 6μs, clock delay at E = 9μs, intrinsic setup time = 2μs and intrinsic clock-to-out time = 3μs. Find out the following:

(i) The setup time required at the input port.

[3 marks]

(ii) The clock-to-out time required at the output port.

[3 marks]

(iii) The clock period and the maximum frequency of the system.

[4 marks]

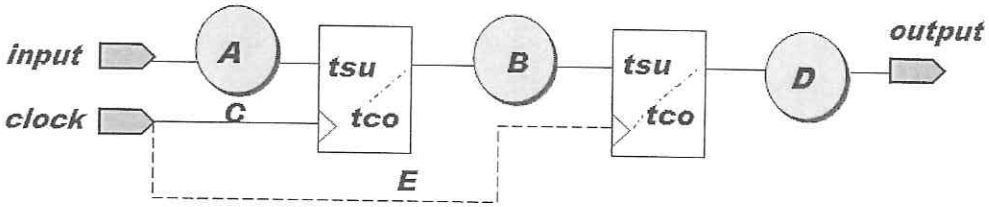

Figure 4a

(c) A Multiple-cycle Synchronizer is given with its flip-flop setup time = 5ns, flip-flop propagation delay = 15ns, τ = 5.8ns, and $T_o = 1.5\times10^{-9}$s. The synchronizer is supplied with 10MHz clock frequency and asynchronous input transition rate 1MHz.

(i) Compute the metastability resolution time, if 1-bit counter is used to divide the input clock signal.

[3 marks]

(ii) What is the mean-time-between-failures of the synchronizer?

[3 marks]

(iii) Calculate the time margin where a failure could occur if the system that consists of the synchronizer is planned for 80 units production.

[3 marks]

End of Paper